"What is included in GUSTECH's Rapid Prototyping Services?"

Since GUSTECH is a '**one-stop-shop**' for all Electronic Hardware, the simple answer is just about everything from **idea-to-working-assemblies**. The provided services are usually simply a function of client need. A few examples (*taken from actual projects completed*) might help:

- A client has a large group of (*software*) programmers but only has one hardware designer who is overloaded and cannot help in a new rush project. GUSTECH is hired to create a board and build 15 prototypes for the programmers to use for testing and modifying their code. The tasks performed included (*a distilled summary without details*):
  - Design circuitry that includes their preferred Microcontroller that interfaces with some of their existing known I/O requirements, add more channels including new analog I/O circuits with Butterworth Analog Filters on the ADC inputs and high-current drivers on the DAC outputs, add remote temperature measurement capabilities, bring all unused Microcontroller I/O pins out to headers for testing and modification purposes, design the complete Microcontroller support circuitry subsystem along with a complete power supply subsystem for the whole board…
  - Write the Technical Interface Specification for all interface requirements for all I/O pins for the Microcontroller so the programmers know how to interface to these pins.
  - Schematic Capture the full design using EAGLE PRO tools.
  - Design a new, high-density, 6-layer Printed Circuit Board.
  - Create the Bill-Of-Materials (BOM) for component purchases.
  - Create a full CAM package for obtaining quotations from at least 20 board manufacturers.
  - Build a spreadsheet for all Board quotations for selecting the winning fabricator.
  - Order the boards (*under a MODC Purchase Order, invoiced at cost – no fees*).
  - Assemble 15 boards, inspect, and check/verify that the power supply and Microcontroller support circuits all work.
  - Deliver full design documentation along with the 15 (partially working, unprogrammed) assembled boards.
- A client has an overworked hardware engineer (sound familiar?) who creates all of the company's board-level products using ExpressPCB without first creating schematics using ExpressSCH. Now they need schematics for the technicians to more easily test the circuits and repair those that do not work properly. The simple task is:
  - Using the ExpressPCB files and hand-built assembly diagrams, reverse-engineer one board's design creating:
    - A schematic using ExpressSCH
    - Create a scalable BOM whose components are selected based upon the intended function and those options
- A client has a 'box' of boards that plug into a backplane that automatically tests a family of products. The test system is vital for maintaining production levels and quality assurance for their products. It has failed recently multiple times due to 'aging' issues, connector issues,

power supply and heat issues, some of them being caused by the repair operations being performed. The client wants the same functionality, but wants to get rid of the many boards filled with 1980's 'popcorn logic' and all of the back-plane interconnections and the huge power supply needed to run it all, including the fans. Fortunately, the client has all the schematics for all the boards, including the backplane, and a crude yet usable interface specification for the connections to their various clamshell test-frames for the products being tested. It is an ALL hardware system; no programming required. This project is a "**<u>Modernization</u>**" Project. What was done:

- Each individual board's schematic was 'captured' into a Xilinx Schematic sheet using hardware blocks that corresponded to each individual 7400-family device, interconnected as defined by the corresponding schematic for each board.
- A top level Xilinx Schematic was created that represented the backplane connections for all of the boards, with a single top-level symbol representing each board in a multi-layer design.
- The entire 'box' of hardware was partitioned and targeted into just two Complex Programmable Logic Devices (CPLD's) that were configured to run at 3.3volt logic.
- An EAGLE PRO schematic was developed capturing the two CPLD's, a simple power supply consisting of 5volts (*for the external I/O interface circuits*) and 3.3volts for the CPLD I/O ports, and 1.8volts for the CPLD core logic using two low-power LDO's, and a simple clock oscillator for circuit operations. The boundary between the CPLD's and the test ports consisted of an array of 3.3volts-to-5volts level translators so that the view on the test cables looked and worked just like the original test 'box'.
- An EAGLE PRO board layout was completed (*4 layers*); a CAM file built; boards bought; parts bought; boards assembled and the CPLD's were programmed.
- Two new test boards were delivered, tested, and found to work perfectly the first time.
- The client now has all of the design files with support documentation so that they can build more 'test' systems in the future, if they wish to. They also are aware that they now also have the ability to make easy-to-implement modifications (*simply by modifying the Xilinx internal design*) to their test systems if the need should arise in the future.

Limitations do exist since the assembly work performed includes all hand-soldering (*supported by 40X power stereo microscope for close-up work*). <u>No ball-grid-arrays</u> are assembled; and when possible they are discouraged from being included in the PC Board layout also since they are very costly to contract-assemble and must be X-Rayed for quality-of-connection and often reworked due to poor assembly yields. The <u>minimum pitch is 0.5mm</u>, simply because the soldering tip and solder are too large for smaller dimensions to provide reliable connections.

Other than these two limitations, all other assembly work has been and is being performed (*for now*). I generally build up to a maximum of 50 assemblies, after which, it is recommended that a contract manufacturer be used for larger quantities to reduce per piece costs.