***S*hock *E*vent *R*ecorder**
Features and Functions

Introduction:

This document briefly presents some of the key features and functions that characterize the Shock Event Recorder (SER), including a general description and modes of operation.

The early versions of this document represent the up-front design goals, while later versions of it, as the design evolves, will more accurately depict achieved goals in the SER. Since this is an on-going design effort, this document is subject to change, at any time.

Contents:

Features:

The SER's features represent a typical set of interface and operational characteristics somewhat similar to those that can be found on any high-end Data Acquisition System (DAS), combined with an additional "value-added" feature set that does not appear to be included on any existing DAS found during the Market Research tasks for the SER development project. The following is a very brief *(not complete*) listing of just some of the more important features of the SER:

- ***Overall***:
  - Built-in non-battery latent power source can run fully operational SER with attached sensors for at least 10 seconds[∞] (*much longer than the total duration of most violent shock events*)
  - Light weight – each SER weighs less than 45 grams[♣]
  - Modular Configuration – each SER completely supports 3 full 4-arm bridge sensor channels; – each SER has four hardware "trigger" inputs which can provide multiple SER's with system-wide fully-synchronized operations
  - Stand-alone autonomous operations using "**e-QUIET**" custom Grey-code sequential state-machine driven activity engines with non-volatile "state" memory
  - Super-ruggedized packaging techniques enable the SER to repeatedly survive extremely violent shock events to 100,000G's[f]
  - Tiny Size – each SER is ≈23 x ≈20 x ≈69 mm[♦] (*about the size of an average man's thumb*) enabling its integration into the tightest of places
- ***Analog Inputs***:
  - 15V/µS Slew Rate
  - 240kΩ typical differential input impedance
  - Bias *(mid-scale)* voltage non-volatile-programmable 0.0V↔+5.0V in 16,384 steps *(305µV/step)*; Pre-boot power-up voltage = 0Volts
  - Designed for broad range of 4-arm piezo-resistive sensors
  - Gain = +0.2V/v Level Translating Wide Bandwidth Difference Amplifier Inputs; subsequent gain stages boost overall gain to more than 4000V/v
  - Input range = ± 10.0V typical; +17.5V ↔ -12.5V Common-Mode Voltage Range
  - Small-Signal Bandwidth *(-3dB)* ≈1.5MHz

[∞] 10 seconds of no-external-power running is subject to change; it is a design goal at this revision level
[♣] Weight is subject to change; it is a design goal at this revision level
[f] 100,000G's survivability is subject to change; it is a design goal at this revision level
[♦] Size is subject to change; it is a design goal at this revision level

- ***Sensor Excitation***:
  - Designed to handle sensor impedances from 120Ω ↔ 3.5kΩ
  - Independent precision non-volatile-programmable voltage sources
  - Maximum current = 43mA for 120Ω sensor excited to +5.191Volts
  - Pre-boot power-up voltage = 2.408Volts *(make sure sensor can handle this)*
  - Sensor Excitation Voltages: +1.507V ↔ +5.191V in 75 discrete, pseudo-logarithmic steps *(14.39mV minimum ↔ 165.9mV maximum / step)*
  - Sensors are controlled by the main sequence engine and are turned on only as needed for given modes of operation
- ***Filtering***:
  - ✓ EMI Protection: -3dB @ 31MHz ⇒ -44dB @ 1.25GHz per input and output wire
  - ✓ ESD Protection: ±8kV *(contact discharge)* Compliance: IEC61000-4-2 (level 4); ±15kV MIL-STD-883, Method 3015 *(Human Body)*
  - ✓ NOTE: same RFI-EMI-ESD protection is also on all digital I/O lines
  - ✓ RFI Protection: -3dB @ 3MHz ⇒ -52dB @ 450MHz per input and output wire
  - ✓ Sensor Anti-Aliasing Filter: 10-pole, DC Accurate, clock tunable Switch Capacitor Linear Phase; up to 40kHz cutoff frequency
  - ✓ Sensor Fixed Back-end Filter: 3-pole Sallen-Key Low-Pass Bessel Filter; *(eliminates clock feed-through from Switched Capacitor Anti-Aliasing Filter)*
  - ✓ Sensor Fixed Front-end Filter: 3-pole Sallen-Key Low-Pass Bessel Filter; 200kHz cutoff
- ***Calibration***:
  - o During-test-Mode: Automatic Shunt Calibration Channel Verification at end of data capture sequence *(stored in data set for post-test survivability verification)*
  - o Pre-test Modes: Host-User GUI adjustment of ALL non-volatile-programmable parameters *(see* Host ⇔ SER *serial communications below)*
  - o Shunt Calibration; per channel; 128 different Ω values across sensor leg from Analog/Sensor Ground to +Signal Input: 100Ω ↔ 10,100Ω each
- ***Digital (trigger) Inputs***:
  - ◊ All four inputs include standard EMI-RFI-ESD protection
  - ◊ Each "change event" is recordable, and all can be used as "triggers"
  - ◊ Four different "hard" trigger (5v) Logic-Level inputs
  - ◊ Inductively Isolated inputs have 100nS maximum propagation delay and an insulation rating = 2.5kV *(UL/CSA/VDE ratings all pending)*
- ***Communications***:
  - ♦ All internal and external communications in serial format
  - ♦ Configuration and mode-profile changes executed within VHDL; configured serially via secure-JTAG communications link; interfaces with design software that is NOT accessible to the user or the HOST system *(for security reasons)*
  - ♦ Host ⇔ SER serial communications = standard serial UART; 19,200 baud fixed protocol *(can be changed to other standards via support equipment)*
  - ♦ SPI and I^2C serial communications used internally

- ***Analog to Digital Conversion***:
    - 16-bit monotonic (no missing codes)
    - All ADC's are "Convert" controlled together for simultaneous sampling of sensor signals, and all data from them is extracted simultaneously
    - Differential Linearity Error: ± 0.5LSB
    - Each ADC has its own buffer-amplifier driver
    - Each ADC has its own precision reference
    - Integral Linearity Error: ± 0.6LSB
    - Maximum throughput: 500kSPS
    - Per channel Successive Approximation Register (SAR) 16-bit Serial Analog-to-Digital Converters (ADC) based upon a (capacitive array) charge redistribution DAC with pseudo differential inputs
    - Sample/Hold Aperture Delay: 2.5nS
    - Sampling rates are clock rate selectable based upon the test scenario requirements, and changes in sampling rates cause corresponding changes in anti-aliasing cutoff frequencies to guarantee no aliasing errors
    - Signal-to-Noise Ratio: 92.7dB
- ***Triggering System***:
    - "hard"
        - All four "hard" trigger inputs are also RFI-EMI-ESD protected
        - Each can create a change on a falling edge
        - Each can create a change on a rising edge
        - Each can indicate a state condition in a high state
        - Each can indicate a state condition in a low state
        - Each selected "event" can cause a mode or sampling change
        - Each selected "event" is recorded at time of event
        - Four inductively isolated discrete digital (5V) logic inputs
    - "soft"
        - Each channel can create an event when its data equals a stored value
        - Each channel can create an event when its data is greater than a stored value
        - Each channel can create an event when its data is less than a stored value
        - Three channels of soft trigger circuits, one per sensor channel
    - "timer"
        - Timer triggers are programmed timed delays for any of the hard and soft triggers listed above, based upon test scenario requirements
    - "Loss of external power" is a unique "hard" trigger source also
    - Any trigger event can cause a change in sampling rate (and its corresponding sensor filter bandwidth), and every trigger is recorded
    - Any trigger event can start the "save-data-pointer" countdown to stop sampling and storing data *(samples-to-go stored value)*, based upon test scenario requirements
    - The prototype version of SER will contain a fixed compliment of hard, soft, and timer triggers for testing purposes only

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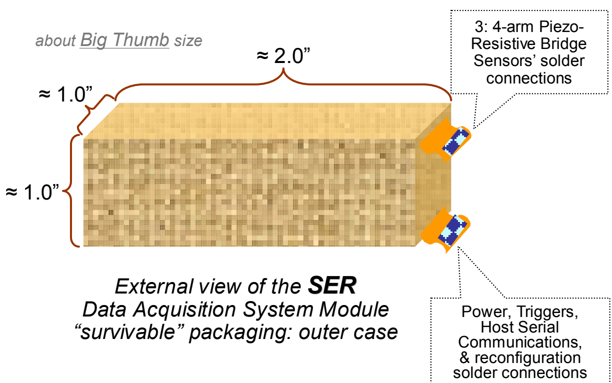
- ***Data Storage***:
  - ❖ A circular buffer is implemented as "cache" storage and the last 524,268 ADC samples are permanently saved @ SAVE ALL, with other data
  - ❖ Saved data has 10 year data retention and unlimited Read/Write cycles coupled with software and hardware write protection schemes
  - ❖ Storage can be enabled *(gated)* or disabled *(blocked)* based upon the *(high or low)* state of any of the "hard" trigger inputs
  - ❖ Storage can be enabled or disabled based upon the data values coming from the ADCs with respect to stored constants *(* $<, \leq, =, \geq, >, \neq$ *tests)*
  - ❖ The "samples-to-go" parameter can be as high as 524,268 ≡ take 524,268 more samples, then stop storing ADC event data, take one last RCAL sample, store system stats, SAVE ALL data and quit
  - ❖ The "samples-to-go" parameter can be as low as zero ≡ stop storing ADC event data, RCAL sample, store system stats, SAVE ALL data and quit
  - ❖ The circular buffer's ring size is 524,268 samples before wrap around
  - ❖ When the "samples-to-go" counter reaches zero, the memory system stores one last RCAL sampling, system stats, does a SAVE ALL, & quits
  - ❖ When the scenario's predefined "save and quit" trigger occurs, the preloaded "samples-to-go" value starts its countdown sequence
  - ❖ When triggered, the ADCs data is written to "cache" memory circular buffer style, interspersed with trigger event data on occurrences
- ***Status Outputs***:
  - ▪ During actual test events, configuration pins are used to post LVCMOS logic levels for "health" and "state" status indications of primary systems *(sampling ADCs, "save and quit" trigger, "samples-to-go" decrementing, power OK, all done)*
  - ▪ During pre-test and post-test operations, the Host system displays status
  - ▪ No extra wire connections are made to the SER to maintain minimum size
- ***Power Requirements***:
  - ✓ 7Vdc minimum ⇒ 16Vdc maximum *(current limited to 200mA)*
  - ✓ External power does not need to be present during actual tests; there is enough internal latent power capacity for ≈ 10 seconds of full power data acquisition and storage activities prior to system auto-shutdown
- ***Connections***:
  - o ALL connections: thru-hole wire solder with dual hole strain reliefs each; soldered holes reliably "survive" extreme shock conditions
  - o One bank of holes: 12 connections *(36 holes total)* to 3 4-arm piezo-resistive sensors (or ground-referenced voltage levels from MEMs)
  - o Other bank of holes: 10 connections *(30 holes total)* for power and ground, Host serial communications, and 4 "hard" triggers with their reference
  - o Tiny, *non-user* "pads": 5 for secure configuration communications
- ***Environmental***:
  - ◊ Humidity *Non-condensing*: 5% ⇔ 95% within operating temperature range
  - ◊ Operating Temperature: 0 – 50^{o}C

- ◊ Single-Axis Shock: 100,000Gs peak, 20µS half sine[⊗]
- ◊ Single-Axis Shock: 40,000Gs peak, 1mS half sine

- ***Survivable Packaging***:
  - ♦ Four distinct protection schemes are being devised to implement a mechanical low pass filter to spread-out the shock wave to a lower average
  - ♦ The circuits are housed 3 dimensionally on a flexible circuit tri-folded
  - ♦ The external box is naturally-shielding carbon composite for light weight and durability *(the box itself is not expected to survive these extreme shocks)*
  - ♦ The internal circuits and cavity are potted with a Jello-consistency compound adhering components to the flex-circuit, giving-in to shocks
  - ♦ The planes of circuits are connected vertically between layers with springs
- ***Physical Characteristics***:
  - o Module Size: 23 x 20 x 69 mm[♠]
  - o Module Weight: 45 grams[♥]

A picture says it better…



*External view of the **SER** Data Acquisition System Module “survivable” packaging: outer case*

General Description:

The SER system is a part of a new generation of compact, technologically advanced, high performance, “unconstrained” Data Acquisition System Modules designed to provide wide bandwidth, high speed digitization and non-volatile data storage from an assortment of sensors during extremely quick, and often environmentally violent test events, including those involving ultra-extreme mechanical impulse shock events and wide bandwidth random vibration conditions.

[⊗] 100,000G’s survivability is subject to change; it is a design goal at this revision level
[♠] Size is subject to change; it is a design goal at this revision level
[♥] Weight is subject to change; it is a design goal at this revision level

It is self-powered for untethered (unconstrained) testing scenarios using the latest in Electrochemical Double Layer Capacitor technology. The analog and digital circuits use high-accuracy, extremely tiny components for minimum mass and maximum performance. The circuitry is protected by both the packaging and the signal line conditioning circuits against large EMI, RFI, and ESD events, which are common phenomenon in many pyro-based testing scenarios.

All user-adjustable parameters are saved on-board in non-volatile memory, including: sensor excitation voltages, RCAL resistance values, mid-scale bias-offsets, gains, cutoff frequencies and sampling rates, and the "save-data" pointer value. Test sequence (mode) profiles are also field-selectable.

Descripton of Operation:

The SER is designed to implement high-end testing functions with the vital features and functions necessary to capture and store the event data with the highest confidence possible using the latest technology and tiniest components available. Minimum mass is a primary goal due to the SER's intended operational testing environment (extremely violent mechanical shocks, etc.). Any extra data-massaging, formatting, and support functions are performed outside the SER to preserve the minimum power and mass needs.

After the SER has been configured for a particular test, and installed as payload in its test article/vehicle and is connected to its sensors, it is "armed" for a single data capture event which will occur as defined by the selected mode of operation and the appropriate sequence of external hard, internal soft, and timer-based triggers.

Each trigger event, including the loss of external power, can change the operational state of the SER, starting the digitization of sensor information, storing the results in the circular buffer, changing the sampling rate and sensor bandwidth midstream as the event profile dictates via the varying trigger occurrences. Generally, the "last" trigger is used to also start the "save-data" pointer countdown sequence, where the internally stored "samples-to-go" parameter determines how many more samples to acquire before permanently saving all of the last 524,268 samples. When sensor-sampling is completed, all channels are placed in RCAL mode, and one sample per channel is also permanently stored as a confidence test for survivability (if RCAL values are good, the rest of the data should be OK also since the circuitry survived the shock event). Each trigger event is also tagged and stored with the sensor data for post-test reconstruction and analysis.

Post-test, the saved data set is serially uploaded to a host computer for archiving, sorting, time-stamping, and analysis purposes.

Modes of Operation:

- Tethered to Host:
  - Channel Setup (adjust all non-volatile-programmable parameters etc.)
  - Sequence Definitions (hard, soft, timer triggers, sampling rates, start-stop events, samples-to-go,etc.)
  - Pretest Readiness (state verification, verify all systems go)
  - Storage Arming (enable non-volatile store and prepare for test)
  - Post-test Data Retrieval (data upload only)
- Untethered (except for external power, or not):
  - Wait for test (armed and running)
  - Real-time Event Recording (saving data)
  - Post-test shutdown (stop-all & remember)

Changes that can selectively change sequence definitions and/or sampling rates include:

- ➢ Loss of external power
- ➢ Change on any of the four external discrete inputs:
  - ❖ High State
  - ❖ Low State
  - ❖ Rising Edge
  - ❖ Falling Edge

  “hard” triggers
- ➢ Data stream value on any of three sensor channels:
  - ✓ Greater than value
  - ✓ Equal to value
  - ✓ Less than value

  “soft” triggers

Timer delays for any of the hard or soft triggers listed above