LIMB RESTRAINT EVALUATOR (LRE)

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ABSTRACT

SRL, under contract to the Air Force Aerospace Medical Research Laboratory (AFAMRL) Biodynamic and Bioengineering Division, has designed, constructed, and tested a Solid State Instrumentation Recorder System for use in a new anthropomorphic dummy system, designed for testing restraint equipment on ejection seats. This totally self-contained instrumentation system is capable of exciting and sensing, in any combination of low level, high level and bilevel sensors, 96 channels of information, at a sample rate of 1000 samples per second per channel. Event data are retrievable from either, or both, on-board storage and standard telemetry.

The system's design rationale will be presented via a brief historical look at previous free-flight instrumentation systems, followed by a detailed presentation of the Limb Restraint Evaluator (LRE).

INTRODUCTION

This paper presents a description of a state-of-the-art data acquisition and recording system which is part of an advanced ejection system test manikin developed by Systems Research Laboratories, Inc. (SRL). The manikin is the Limb Restraint Evaluator (LRE), which was designed to test restraint devices to be incorporated into modern aircraft ejection equipment by the U.S. Air Force. The program was sponsored by the Air Force Aerospace Medical Research Laboratory (AFAMRL) and the Life Support System Program Office of the Aeronautical Systems Division.

This discussion essentially consists of two parts. Following a brief statement of the need, a description of the numerous technical challenges associated with manikin data acquisition system design are presented. The second part of the paper describes how these challenges were addressed in designing and implementing the LRE instrumentation system.

THE TASK

The design goals of the LRE presented a demanding instrumentation challenge when one considers historical systems. The primary task involved successfully sensing and capturing data for 96 phenomena sources for a free-flight test article for the ACES II restraint tests. The system had to be totally self-contained and able to operate under harsh physical and environmental conditions. It had to be generic to accommodate future program requirements, modular for ease of expansion and repair, high in density due to space limitations, and as reliable as possible.

SOME HURDLES

The large number of data channels presented the first challenge. Typical tests in the past involved using a frequency modulation (FM) technique of encoding data on a telemetry link carrier to acquire free-flight test data. A major drawback with this technique is that it severely limits the number of channels that can be used per transmitter carrier frequency. One solution is to increase the number of transmitters introducing additional problems concerning antennae locations. A better solution is to change the data encoding technique to a Pulse Code Modulation (PCM) type system (time multiplexed).

While the use of a PCM system for the conversion of analog signals to a digital format suitable for data capture operations solves the channel capacity problem, a new problem related to the time sampling technique is presented. One must be aware of the introduction of aliasing errors when using any form of time-sliced sampling techniques. In the frequency domain, there is a region called frequency overlap, where the folding frequency, which is one-half of the sampling frequency, crosses down into the spectrum of the signal to be sampled. Aliasing errors may result if the overlap region is not suppressed, and can be done by either increasing the sampling frequency sufficiently beyond twice the frequency content of the channel sensor's spectral content, or that channel's signal content can be band-limited with an in-line low pass filter.

A low pass filter is used to reduce man-made electrical interference noise, to reduce electronic noise and, of course, to limit the bandwidth of the signal for sampling purposes. Electronic noise is random noise with noise power proportional to bandwidth and is present in transducer resistances, like four arm strain bridges, piezoresistive accelerometers, and potentiometric position sensors, as well as in circuit resistors,

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and in active solid state devices themselves. Power supply noise, especially from DC to DC converters and switchers, are also a primary source of noise when used as sources for sensor excitation. The high frequency "noise" sources can generate errors in the real information desired from sensors in this type of system, but can be effectively removed with a low pass filter in-line for each channel. Having established the need for antialiasing (presampling low pass) filters, the type of filter that should be used is typically of the "Butterworth" class. A "Bessel" type low pass filter is used where the signal amplitude fidelity is of little importance compared to the necessity for linear phase response. Since sensor signal amplitude represents the magnitude of the physical phenomena, which is the desired data in most of these tests, a "Butterworth" type filter is typically used, since it is characterized by a maximally flat amplitude response in the passband.

Telemetry dropout presents another challenge. The total losses in the test data radio link can be due to any one or combination of several potential problems. The most common is the random flight nature of the test article causing the transmitter antenna to lose it proper orientation with respect to the data retrieval antenna(e). Also, atmospheric noise interference is a common cause for telemetry "dropout." The transmission can also be distorted by multipath transmissions (and echoes) through rocket plumes and off of local poles and buildings. Total momentary telemetry "dropout" can also be the symptom of a main power relay contact opening if there is insufficient capacitance in the power source for the analog-to-digital conversion system or the transmitter. Relay contact chatter (bounce) or separation can easily occur due to wide spectrum and large amplitude vibrations imposed on the system during the rocket sled rail travel time and during large acceleration impulse periods (ejection, wind blast, and main chute deployment). A combination of techniques can solve and/or circumvent most of the telemetry data "dropout" problems. Data capture probability is enhanced by using more than one receiving station. Trailer mounted receivers and recorders in a triangular pattern surrounding the test area has proven to be more reliable than a single fixed receiving station designed to work as a general receiver for the entire test site. Another possible technique involves mounting a second transmit antenna along an arm, or better still, along a leg of the test manikin. Another solution might be to drive the second antenna with a separate transmitter operating at a different frequency. This, however, doubles the number of receiving stations and data to be analyzed, thus increasing test costs. However, even if this second telemetry link is used, data dropout can still occur due to general swamping by atmospheric noise. A solution to dropouts caused by short term atmospheric noise might be to delay the telemetry serial data bit stream to the second telemetry link for a fixed time delay via a long shift register, hoping that the data dropout period is shorter than the time delay between data transmissions. These techniques, as well as others, can at least limit the dropout problem, if not eliminate it. Another serious consideration involves using on-board storage as a back-up data capture technique.

Before an on-board storage technique can be selected, several important system parameters must be analyzed. The system sample/data rate and the total capture time or volume of data are the most important. An ideal on-board memory subsystem would be nonvolatile and have high density (high memory capacity for its volume), lower power requirements, and fast read/write speeds. Due to limitations in one or more parameters, certain compromises must be made when using currently available memory technologies. One memory device currently being implemented as a piggy-back memory system to an existing free-flight test apparatus, uses "bubble memory" technology. While this nonvolatile system has fairly high density properties, its slow read/write speeds, high power requirements, high software overhead (housekeeping) requirements, and its limited environmental tolerance capacity made it a poor candidate for the LRE system. Other nonvolatile memory devices commercially available include Programmable Read Only Memories (PROMs), Erasable Programmable Read Only Memories (EPROMs), Electrically Erasable Programmable Read Only Memories (EEPROMs), Electrically Alterable Read Only Memories (EAROMs), and variations of these types of memories. Most of these devices have all the desirable attributes of the "ideal" memory except for their very slow read/write speeds. Static Random Access Memories (SRAMs) are fast, use little power, and can handle harsh environments, but they currently have insufficient density and, most importantly, they are volatile devices. Dynamic Random Access Memories (DRAMs) have all the desirable features of the "ideal" memory, except for the loss of memory with the loss of power problem.

Another problem that occurs when increasing the number of data channels concerns implementation of adequate portable power source. The requirement for more channels means more sensors, more electronic instrumentation for signal conditioning, more weight and space, and more internal heat dissipation. Most batteries lose capacity as temperature increases, creating a need for oversize batteries. To add to the problem, there does not appear to be any well documented empirical data of the temperature/time profile within a fully operational and enclosed ejection test dummy operating under these extreme test conditions.

Another temperature related problem is dealt with easily using current technology. In the past, off-the-shelf operational amplifiers were used for signal conditioning, mainly because they were cheaper and readily available. True instrumentation amplifiers, while ideal for this task, have in the past been hybrid devices which were large, expensive, and power hungry. The use of monolithic instrumentation amplifiers virtually eliminates temperature variations in the signal conditioning section of the system. True instrumentation amplifiers are also preferred because of their high common mode rejection capabilities, low offset errors, high gain capacities, and a host of other "ideal" features.

Another potential temperature related problem can develop with the newly introduced low pass filters. The most common type of low pass filters currently in use today are low pole filters built around operational amplifiers. These have the advantage of eliminating the need for fairly large and heavy inductors that would normally be required to implement equivalent (and inefficient) resistor/inductor/capacitor filters followed by amplifiers for the same operational characteristics. Keeping in mind that every sensor channel needs an antialiasing filter, where an active filter could easily involve using two integrated circuits and a dozen discrete components for each channel, the 96 channel system presents major complexities in the form of power and packaging requirements. The cut-off frequency of such a filter is a function of the resistors and capacitors in each circuit. If ratings with 1 percent accuracy were chosen for the resistors and capacitors (difficult to do for capacitors) for a four pole low pass Butterworth filter, the cut-off frequency from one such filter to the next could easily differ by as much as 10 percent from compounding errors, which is fairly significant in most signal spectrums. A total new circuit design is required whenever a different filter cut-off frequency is desired. The worst problems are instability and drift due mainly to temperature changes causing changes in circuit capacitance. Unless very expensive resistors and capacitors with nearly constant temperature response characteristics are used, temperature drift errors cannot be eliminated using operational amplifiers as the base for our antialiasing low pass filters.

There are many other problems associated with this system, which are too numerous to cover adequately within the scope of this presentation. LRE system improvements were adapted to remedy most of these problems. Some problems, like telemetry dropout, will still occur, even in the LRE system. Some system problems, like data format inconsistencies between testing agencies, and final data formatting and analysis and their related inaccuracies are out of the scope of LRE development, and yet they have a real impact on the final test results.

SOLUTIONS

Referencing Figure 1, one can readily note the dual data capture paths involving both telemetry and internal (on-board) memory. As in most similar systems, the PCM is the heart of this technique, in that it performs the actual data acquisition activities.

The primary purpose of a PCM system is the conversion of many incoming analog signals to a serial digital representation of those signals. A typical PCM system contains a multichannel analog signal multiplexer (multiposition electronic switch), a signal sample-hold circuit, a high speed successive approximation analog-to-digital converter, a parallel-to-serial digital signal

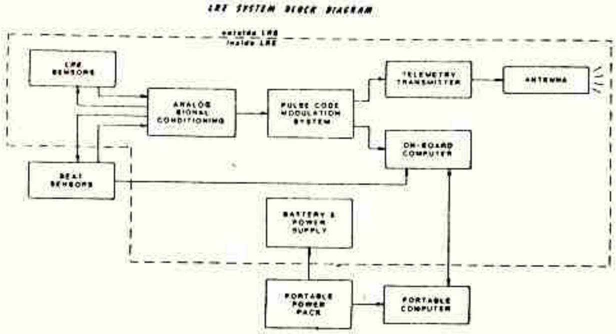

Figure 1. LRE System Block Diagram

converter, necessary timing and control signals, a well regulated internal power supply subsystem, and a transmitter low pass filter circuit. All front-end interface circuits for the LRE PCM system are of the high level variety. This is due to the need to boost all signal levels to high level signal strength for proper filtering prior to being sampled by the PCM system. The PCM system chosen was an EPROM driven hard logic controller type, allowing for easy changes in sampling order and sampling rates via subcommutation and supercommutation techniques.

One output from the PCM system is a "Bessel" (linear phase) filtered NRZ-L bit stream which is then sent to an on-board telemetry (UHF) transmitter. The transmitter signal is then sent to a skull mounted antenna. In the past, serious problems have occurred involving Radio Frequency Interference (RFI) coupling of the transmitter's signal to the sensor inputs to the system. This problem can manifest itself in many ways, the most common being large noise and intermodulation signals and large DC bias (offset) errors. It is usually caused by an improperly shielded transmission cable (from the transmitter to the skull antenna), and by an improperly tuned (mismatched) system which results in "RF" emissions from the transmission cable being absorbed by anything close to the cable, such as sensors and low level circuitry. To circumvent some of these problems in the LRE, all low level circuitry is enclosed in the all metal spine, which is at ground potential. All sensor cables are grounded at the sensor source to that same spine ground point. The antenna cable will be double shielded, and the antenna will be tuned for maximum signal strength, resulting in minimum cable emissions.

Another group of signals from the PCM system are sent to the on-board computer system. They are the NRZ-L data bit stream and associated clocks and synchronization signals. These signals are converted into a parallel format suitable for storage within the on-board computer. The primary elements of the on-board computer are the Central Processing Unit (CPU), PCM interface unit, DRAM array and its controller, communication and I/O ports, and assorted "glue" ICs. The primary task of the CPU, during the data capture process, is to move new PCM data from the PCM interface unit to the DRAM array for storage, and to keep track of how much storage is available for this process. Prior to the data capture process, the CPU, via the EPROM stored program, checks the entire system for operational readiness, properly sequences the LRE system power, and runs a full calibration check on the low level channels in the system. Following data capture, the CPU shuts down all power within the LRE, except for itself, and then continuously dumps the DRAM array contents to an external computer. The CPU used is the 68000 unit, which was chosen for its high speed and continuous memory capacity. It is run synchronized to the PCM interface board during the data capture process for maximum efficiency and reduced turnaround time. The communications and I/O section consists of both a serial (RS-232C) port and an IEEE-488 port, as well as control input lines and status output lines. The current software package utilizes the RS-232C port for status reports and the data dumps, but software could be written to implement the high speed parallel port for those tests that warrant its use. The PCM is currently set up to capture 96 channels of sensor information at a 1000 samples per second per sensor rate, with four additional bytes of information per scan, which yields data at a rate of 100,000 bytes of information per second to be stored. The DRAM array is large enough to continuously capture about 5 1/4 seconds of sensor data, which is more than adequate for the tests for which the LRE was designed. The PCM interface unit is a serial-to-parallel conversion system with interface circuitry for the CPU. Much of the computer system is implemented with high speed CMOS logic to reduce power needs and heat generation. Where higher speed is needed, Programmable Array Logic ICs (PALs) were used to increase the density of the system (by implementing the functions of several "glue" ICs in just one IC). The computer system is housed in a metal case on eight small printed circuit boards sitting on a motherboard.

The analog signal conditioning subsystem, as depicted in Figure 2, excites all sensors, and converts their signals to the proper levels to be sampled by the PCM system. There are four main elements in this section: low level interface, high level interface, bilevel interface, and the presample antialiasing low pass filters. All signals entering the filters have the same peak amplitude range (high level signals) for maximum accuracy through the filters. The low level interface boards are typically used to boost the signals from strain gauge bridges and piezoresistive accelerometers to the levels required by the filters and the PCM. They feature monolithic instrumentation amplifiers, adjustable gain and offset precision resistors, and a computer controlled "RCAL" offset calibration mode for each channel. Each channel has its own buffered and filtered excitation source for maximum isolation from other channels. The high level interface board features individually buffered and filtered excitation for all of the potentiometric position sensors within the LRE. Fixed resistors are

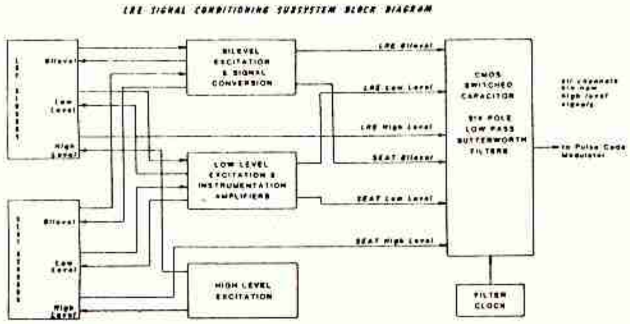

Figure 2. LRE Signal Conditioning Subsystem Block Diagram

chosen for maximum sensitivity for each channel. The bilevel interface board accepts go/no-go information (switch contacts and logic levels typically) information from the LRE, the ejection seat, and the velocity harp, and converts these signals, in groups of six at a time, into high level signals suitable for the filters and the PCM.

The presampling antialiasing Butterworth low pass filters are of the sixth order CMOS switched capacitor technology. There are no capacitors or resistors to tune the cut-off frequency since that is a function of an external clock frequency, thereby circumventing all the usual associated temperature drift errors. In addition, the cut-off frequencies of all 96 channels are tracked together at the same frequency since they are driven from a common clock. The filter clock shown in Figure 2 is implemented as a fully redundant failsafe clock system, because the loss of the filter clock means the loss of all data. This filter clock board also contains circuitry to monitor the state of the filter clock, with an analog representation of the clock frequency being monitored by the PCM, as well as identification of which clock is driving the filters. This board also contains circuitry which reports the status of the system power supply, as well as the temperature in the spine box.

The LRE system power supply consists of three main elements: the battery, the DC to DC converter, and the power switch relays. The battery is a wired Silvercell array designed to provide maximum power capacity for the entire system. The Silvercell has a fairly unique advantage in that capacity increases with rising temperature, and it has extremely high power/volume and power/weight ratios when compared with other rechargeable battery technologies. The DC to DC converter provides well regulated power for all sensor excitation buffer circuits, the instrumentation electronics, and the computer. It uses high efficiency switching technology, and all input and output voltage lines have EMI/RFI filters in-line. All power, except for the computer power, is switched, by individual voltages, by high power VMOSFET solid state relays. These relays provide a computer controllable means of conserving power while eliminating blackout or brownout faults due to power relay contact bounce.

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